REMARKS

Reconsideration and allowance of the above-identified application are respectfully requested.

Claims 2-7, 9-14, 16-19, 21-43 are currently pending, wherein claims 3, 4, 7, 10, 11, 14, 16-19, 21, 22, 24, 28 and 32 are independent. Claims 2-4, 6, 7, 9, 10, 11, 13, 14, 16-19, 21 and 22-24 have been amended. Claims 1, 8, 15 and 20 have been canceled. Claims 36-43 have been added. No new matter has been introduced by way of these new claims.

Applicant notes with appreciation the acknowledgment by the Patent Office of the Information Disclosure Statement previously submitted to the Patent Office.

Applicant further notes with appreciation the acceptance of the drawings filed on November 16, 2001.

Applicant notes with appreciation the allowance of claims 28-35.

Applicant also notes with appreciation the characterization of claims 11, 12 and 22-27 as being allowable if rewritten or amended to overcome the rejections under 35 U.S.C. § 112, second paragraph, set forth in the present Office Action.

Applicant further notes with appreciation the characterization of claims 3-5, 7, 10 and 14 as being allowable if rewritten in independent form. Applicant hereby amends claims 3, 4, 7, 10 and 14 merely to write these claims in independent form, including all of the limitations of the base claim and any intervening claims. These amendments do not narrow or otherwise limit the scope of the claims, are not made for any purpose related to patentability, and are fully supported by the present application. No new matter has been introduced by way of these amendments. It is respectfully submitted that claims 3, 4, 7, 10

and 14 are allowable. Applicant respectfully notes that claims 2, 5, 6, 9, 13, 36-39, 42 and 43 variously depend from claims 3, 4, 7, 10 and 14, and are, therefore, also allowable.

Applicant would like to thank Examiner Gopal C. Ray for the personal interview conducted on November 4, 2004. In compliance with M.P.E.P. § 713.04, the substance of that interview is incorporated in the foregoing amendments to the claims and in the following remarks.

In the fourth section of the Office Action, claims 16-19 and 21 are objected to under 37 C.F.R. § 1.75(c), as allegedly being of improper dependent form for failing to further limit the subject matter of the previous claim. Applicant hereby amends claims 16-19 and 21 merely to write these claims in proper independent form, including all of the limitations of the base claim and any intervening claims (Applicant respectfully notes that original claim 21 should have depended from original claim 20). These amendments do not narrow or otherwise limit the scope of the claims, are not made for any purpose related to patentability, and are fully supported by the present application. No new matter has been introduced by way of these amendments.

In the fifth section of the Office Action, claims 11, 12, 16, 17 and 22-27 are rejected under 35 U.S.C. § 112, second paragraph, for alleged indefiniteness.

In particular, the Patent Office asserts that in claim 11, lines 1-2, the phrase "the means for network controlling" lacks proper antecedent basis, because "means for network interfacing" has been claimed earlier. Applicant hereby amends claim 11 to change the phrase "means for network controlling" to "means for network interfacing." Claim 11 has also been amended merely to write the claim in independent form. It is respectfully

submitted that claim 11 is allowable. Applicant respectfully notes that claims 12, 40 and 41 depend from claim 11, and are, therefore, also allowable.

The Patent Office further asserts that in claim 16, lines 1-2, the phrase "the serial mass data storage host adapter" lacks proper antecedent basis, because "a serial ATA host adapter" has been claimed earlier. In addition, in lines 2-3, the phrase "the high speed mass data storage unit" lacks proper antecedent basis, because "a data storage unit" has been claimed earlier. Applicant hereby amends claim 16 to change "serial mass data storage host adapter" to "serial ATA host adapter" and to change "high speed mass data storage unit" to "data storage unit." Claim 16 has also been amended merely to write the claim in independent form.

The Patent Office further asserts that the feature of "wherein the network controller includes an Ethernet controller" recited in claim 17 was already claimed. Applicant hereby amends claims 17 and 18 to recite the that the "high speed Ethernet network controller has an operating speed of at least 1 Giga Bit per second" and "the high speed Ethernet network controller includes a MAC layer and a physical layer," respectively. Claims 17 and 18 have also been amended merely to write these claims in independent form.

In addition, the Patent Office asserts that in lines 1-2 of each of claims 22 and 23, the phrase "the high speed Ethernet controller" should be changed to "the high speed Ethernet network controller," because of an alleged lack of proper antecedent basis. Applicant hereby amends claims 22 and 23 to change the "high speed Ethernet controller" to the "high speed Ethernet network controller." Additionally, claim 22 has been amended merely to write the claim in independent form (Applicant notes that original claim 22 should have depended

from original claim 20). It is respectfully submitted that claim 22 is allowable. Applicant respectfully notes that claim 23 depends from claim 22, and is, therefore, also allowable.

The Patent Office asserts that in claim 24, lines 7, 8, 11 and 12, the phrase "the high speed bus interface" lacks proper antecedent basis, because "means for bus interfacing" has been claimed earlier. Applicant hereby amends claim 24 to replace the phrase of "high speed bus interface" with "bus interfacing means." It is respectfully submitted that claim 24 is allowable. Applicant respectfully notes that claims 25-27 variously depend from claim 24, and are, therefore, also allowable.

These amendments do not narrow or otherwise limit the scope of the claims, and are fully supported by the present application. No new matter has been introduced by way of these amendments.

Accordingly, reconsideration and withdrawal of these grounds of rejection of claims 11, 12, 16, 17 and 22-27 are respectfully requested. It is respectfully submitted that claims 11, 12 and 22-27 are allowable.

Additionally, Applicant respectfully submits that independent claims 16-19 and 21 are allowable, as all objections and rejections with respect to these claims have been overcome.

Furthermore, Applicant respectfully notes that claim 16 recites features similar to those recited in allowable claims 3 and 10, including the allowable features stated by the Patent Office in the Examiner's Statement of Reasons for Allowance. [*see* Office Action, page 6] Applicant also respectfully notes that claim 17 recites features similar to those recited in allowable claims 4, 11, 22, 26, 29 and 33. Applicant further respectfully notes that claim 18 recites features similar to those recited in allowable claims 5, 12, 23, 27, 30 and 34. Additionally, Applicant respectfully notes that claims 19 and 21 recites features similar to

those recited in allowable claims 7, 14, 25, 31 and 35. Therefore, it is respectfully submitted that independent claims 16-19 and 21 are allowable for these additional reasons.

During the interview, the rejection of claims 1, 6, 8 and 13 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Kumar et al. (U.S. Patent No. 5,970,069, hereinafter "Kumar") in view of Hannah et al. (U.S. Patent No. 5,809,337, hereinafter "Hannah") was discussed. No agreement was reached. These rejections are respectfully traversed.

To facilitate progress in the prosecution in the present application, Applicant hereby cancels claims 1 and 8, and amends claims 6 and 13 to depend from allowable claims 3 and 10, respectively. It is respectfully submitted that claims 6 and 13 are allowable. Applicant reserves the right to file one or more continuation applications directed to the canceled claims.

Although claims 1 and 8 have been canceled, Applicant respectfully asserts that claims 1 and 8 are nonetheless allowable for the following reasons.

Conventional systems typically include a parallel ATA host adapter within a core chipset. In addition, the trend in conventional systems is to integrate an increasing number of function into fewer semiconductor devices such as the core chipset. [*see* present application, page 5, paragraph 0015] As illustrated in Figure 2 of the present application, the present invention recognizes the advantages of not including the serial ATA host adapter 36 in the core chipset 22, but instead including the serial ATA host adapter 36 in a multi-port communications chip 20. Serial ATA operates at a significantly higher data rate than parallel ATA, making the serial ATA host adapter 36 more suitable for fabrication with mixed-signal CMOS processes than fabrication processes typically employed for the core chipset 22. Including the serial ATA host adapter 36 in the core chipset 22 would potentially increase

costs due to more complex fabrication methods and possibly lower yield. Instead, the serial ATA host adapter 36 is fabricated in a semiconductor device outside of the core chipset 22, which can result in faster time-to-market, improved yield, and lower cost. [*see* present application, page 5 – page 6, paragraph 0015]

In addition, the serial ATA host adapter 36 is combined with the high speed Ethernet controller 33 into a single semiconductor device separate from the core chipset 22. Combining the serial ATA host adapter 36 and the high speed Ethernet controller 33 into a single, separate semiconductor device can decrease cost by combining functions that have similar fabrication requirements, reduce the required board area, and minimize chip count. [*see* present application, page 6, paragraph 0015]

Also, in a preferred embodiment, recognizing that a single high speed bus 30 can support both the serial ATA host adapter 36 and the high speed Ethernet controller 33 through a single bus interface 28 leads to the elimination of a separate bus interface and bus for each function. Older technologies, such as PCI (Peripheral Component Interface), do not have sufficient bandwidth on a single bus to adequately support both a storage device and network controller with present-day multimedia requirements. Using a single bus interface 28 to interface both the serial ATA host adapter 36 and the high speed Ethernet controller 33 to the high speed bus 30 further reduces complexity which can lead to further cost reduction, improved yield, and reduction in required board area. [*see* present application, page 6 – page 7, paragraph 0015]

Kumar discloses a *single chip* integrated remote access processor that includes a plurality of communication interface units. [*see* Kumar, column 1, lines 59-64] A data routing control circuit is coupled to the plurality of communication interface units. The data

routing control circuit includes an internal transfer bus, a multi-channel direct memory access (DMA) controller, a central processing unit (CPU), an internal memory, a local memory interface, a local memory controller and a bridge circuit. [*see* Kumar, column 2, lines 1-5] The internal transfer bus is coupled to the DMA controller, CPU, local memory controller and bridge circuit for passing data, address and control information to and from the various elements. According to Kumar, "[t]he single chip integration enables high performance and low cost." [Kumar, column 2, lines 26-27]

As acknowledged by the Patent Office, Kumar does not disclose or suggest the feature of "a serial mass data storage host adapter in communication with the high speed bus interface to control a high speed mass data storage unit." In addition, it is respectfully submitted that Kumar does not disclose or suggest the feature of "a high speed bus interface to interface to a core chipset through a high speed bus." Kumar discloses that the single chip integrated processor includes a PCI unit. [*see* Kumar, column 1, lines 59-64] It is respectfully noted that PCI is *not* a high speed bus interface. As discussed previously, older technologies, such as PCI, do not have sufficient bandwidth on a single bus to adequately support both a storage device and network controller with present-day multimedia requirements. It is additionally noted that the elements of the processor 34 reside on a *single chip*. Therefore, not only does Kumar not disclose a high speed bus interface, it is respectfully submitted that Kumar does not disclose the feature of a high speed bus interface *to interface to a core chipset through a high speed bus*, or a network controller *in communication with the high speed bus interface* to control a network port.

In complete contrast to Kumar, the serial mass data storage host adapter according to exemplary embodiments is included in a separate multi-port communication chip that is

interfaced to the core chipset though a high speed bus. Including the serial mass data storage host adapter in the core chipset would potentially increase costs due to more complex fabrication methods and possibly lower yield. Instead, the serial mass data storage host adapter is fabricated in a semiconductor device *outside* of the core chipset, which can result in faster time-to-market, improved yield, and lower cost. In addition, it is respectively submitted that Kumar does not disclose or suggest a *single* high speed bus and a high speed bus interface to support *both* a serial mass data storage host adapter and a network controller.

Hannah discloses a mass storage device having a storage medium on which digital signals can be stored. The mass storage device is coupled to a computer through a high-speed serial bus. The high-speed serial bus has a latency and a signal transmission rate sufficient to enable transmission of digital signals between the mass storage device and the computer without interim storage of the digital signals in a buffer inside the mass storage device. The computer has a processor capable of processing the digital signals and the digital signals can be transmitted between the mass storage device and the computer without processing of the digital signals by a processor in the mass storage device. [*see* Hannah, column 2, lines 26-33]

It is respectfully submitted that Hannah does not disclose or suggest the feature of a serial mass data storage unit adapter. Hannah discloses the high-speed serial bus 25, but nowhere does Hannah disclose, discuss, or even suggest a serial mass data storage host adapter. For example, the Patent Office's citation of Hannah to supposedly disclose the feature of a serial mass data storage host adapter merely discloses the high-speed serial bus 25.

In addition, it is respectfully submitted that Hannah does not disclose a *single* high speed bus and a high speed interface to support *both* a serial mass data storage host adapter and a network controller. Hannah merely discloses that the high-speed serial bus 25 is coupled between a mass storage device and a computer for sending digital signals between the mass storage device and the computer at a rate sufficient for high performance input/output. [*see* Hannah, column 3, lines 3-6] In contrast to Hannah, according to exemplary embodiments of the present invention, recognizing that a single high speed bus can support both the serial mass data storage host adapter and the network controller through a single bus interface leads to the elimination of a separate bus interface and bus for each function. Using a single bus interface to interface both the serial mass data storage host adapter and the network controller to the high speed bus further reduces complexity which can lead to further cost reduction, improved yield, and reduction in required board area.

Therefore, it is respectfully submitted that Hannah does not address the above-identified deficiencies of Kumar.

Furthermore, according to M.P.E.P. § 2143, to establish a prima facie case of obviousness, three basic criteria must be met. "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." [M.P.E.P. § 2143] In other words, "[o]bviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art." [M.P.E.P. § 2143.01] As neither Kumar nor Hannah disclose or suggest numerous

features of the present invention, it is respectfully submitted that there is there is no teaching, suggestion or motivation, either explicitly or implicitly, to combine the references in the manner suggested by the Patent Office. Consequently, it is respectfully submitted that the Patent Office has not established a prima facie case of obviousness. For at least the aforementioned reasons, it is respectfully submitted that the combination of Kumar and Hannah does not render independent claims 1 and 8 unpatentable.

Furthermore, according to M.P.E.P. § 2142, "[t]o reach a proper determination under 35 U.S.C. 103, . . . impermissible hindsight must be avoided and the legal conclusion [of obviousness] must be reached on the basis of the facts gleaned from the prior art." Furthermore, according to M.P.E.P. § 2143.01, "[t]he mere fact that references can be . . . modified does not render the resultant combination obvious unless the prior art also suggests the desirability of [such modification]." [citing *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990)] Since the Patent Office has offered no proper support or motivation for combining the references, it is respectfully submitted that the rejection based on obviousness is founded upon "knowledge gleaned only from applicant's disclosure." [*see* M.P.E.P. § 2145] Consequently, it is respectfully submitted that the rejection entails hindsight and is, therefore, improper.

For at least the foregoing reasons, it is respectfully submitted that the combination of Kumar and Hannah does not render the subject matter of independent claims 1 and 8 obvious.

During the interview, the rejection of claims 2, 9, 15 and 20 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Kumar in view of Hannah and further in view of the common knowledge in the art was discussed. No agreement was reached. These rejections are respectfully traversed.

To facilitate progress in the prosecution in the present application, Applicant hereby cancels claims 15, and 20, and amends claims 2 and 9 to depend from allowable claims 3 and 10, respectively. It is respectfully submitted that claims 2 and 9 are allowable. Applicant reserves the right to file one or more continuation applications directed to the canceled claims.

Although claims 15 and 20 have been canceled and claims 2 and 9 are allowable, Applicant respectfully asserts that claims 2, 9, 15 and 20 are nonetheless allowable for the following reasons.

It is respectfully submitted that nowhere does either Kumar or Hannah disclose a serial mass data storage host adapter that is a serial ATA host adapter. As acknowledged by the Patent Office, Kumar does not even disclose a serial mass data storage host adapter. Furthermore, Hannah merely discloses a high-speed serial bus. It is respectfully submitted that *nowhere* does Hannah disclose or suggest a serial mass data storage host adapter, and does not disclose or suggest a serial ATA host adapter or even serial ATA technology.

It is respectfully submitted that *nowhere* does the common knowledge in the art disclose or suggest the feature of a *single* high speed bus and a high speed interface to support *both* a serial mass data storage host adapter and a network controller, in particular, in which the serial mass data storage host adapter is a serial ATA host adapter. Contrary to the assertions of the Patent Office, the background of the present application merely states that "a new standard (Serial ATA) for interconnecting computer systems to internal storage units has been proposed." [present application, page 1, paragraph 0002] It is respectfully submitted that the background does not disclose or suggest the feature of a *single* high speed bus and a high speed interface to support *both* a serial mass data storage host adapter and a network

controller, in particular, in which the serial mass data storage host adapter comprises a serial ATA host adapter.

Furthermore, the Patent Office states that "[i]t would have been an obvious choice of design to one of ordinary skill in the art at the time the invention was made to include the [feature of a serial ATA host adapter] in the system of Kumar et al. because these are alternatively replaceable elements that can be utilized to accomplish particular objective [sic] in order to fulfill system requirement [sic]." As neither Kumar nor Hannah nor the common knowledge in the art disclose or suggest numerous features of the present invention, it is respectfully submitted that there is there is no teaching, suggestion or motivation, either explicitly or implicitly, to combine the references in the manner suggested by the Patent Office. Rather, it is respectfully submitted that the rejection entails hindsight and is, therefore, improper.

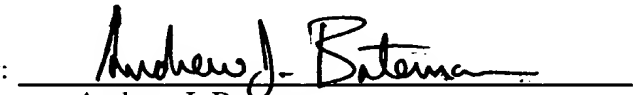
In addition, during the interview, the Patent Office asserted that a combination of Figure 1 of the present application and the reference "Serial ATA: High Speed Serialized AT Attachment" (dated August 29, 2001, previously submitted in the IDS, hereinafter the "Serial ATA reference") could render the subject matter of claims 2, 9, 15 and 20. *Even if* such a combination were proper, it is respectfully submitted that such a combination does not disclose or suggest numerous features of the present invention, including the feature of a *single* high speed bus and a high speed interface to support *both* a serial mass data storage host adapter and a network controller, in particular, in which the serial mass data storage host adapter is a serial ATA host adapter.

For at least the foregoing reasons, it is respectfully submitted that the combination of Kumar, Hannah and the common knowledge in the art (or the combination of Figure 1 of the

present application and the Serial ATA reference) does not render the subject matter of claims 2, 9, 15 and 20 obvious.

All of the objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the present application is in condition for allowance and a notice to that effect is earnestly solicited. Should the Examiner have any questions regarding this response or the application in general, the Examiner is urged to contact the Applicant's attorney, Andrew J. Bateman, by telephone at (202) 625-3547. All correspondence should continue to be directed to the address given below.

Respectfully submitted,

By: 

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